15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

FEATURES

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V-15V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 16-mΩ Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Integrated 33KHz~133KHz programmable frequency clock generator with ±2% accuracy
- Integrated amplifier for silicon photodiode signal demodulation
- Input Under-Voltage Lockout
- Over Current Protection
- Over Temperature Protection
- 3mm*3mm QFN-15L Package

APPLICATIONS

- General Wireless Power Transmitters
- Proprietary Wireless Transmitters

DESCRIPTION

The SCT63141 is a highly integrated Power Management IC allows achieving high performance, high efficiency and cost effectiveness of wireless power transmitter system to support up to 15W power transfer.

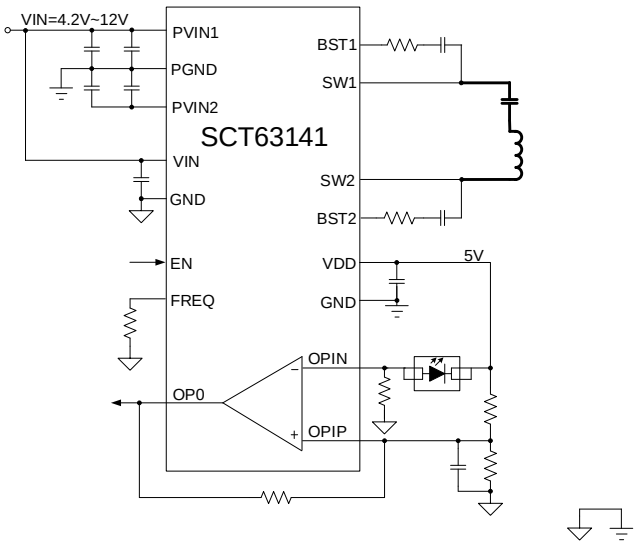
This device integrates a 5V-LDO, 4-MOSFETs full bridge power stage，gate drivers, a high-precision 50% duty clock generator with programmable frequency for configuring the transmitter's output power easily, and also an amplifier for silicon photodiode signal demodulation to provide total solution with single chip.

The proprietary gate driving scheme optimizes the performance of EMI reduction to save the system cost and design. The build-in 5V low dropout regulator LDO can provide power supplies to external circuitries.

The SCT63141 features input Under-Voltage Lock-out UVLO, over current, short circuit protection, and over temperature protection.

The SCT63141 is available in a compact 3mm*3mm QFN package.

TYPICAL APPLICATION



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update DEVICE ORDER INFORMATION

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT63141FMAR	Tape & Reel	5000	3141	15	QFN-15L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	24	V
PVIN1, PVIN2	-0.3	17	V
SW1,SW2	-1	17	V
BST1,BST2	-0.3	23	V
BST1-SW1,BST2-SW2	-0.3	6	V
VDD, ISNS, EN, FREQ, OPIP, OPIN, OPO	-0.3	6	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

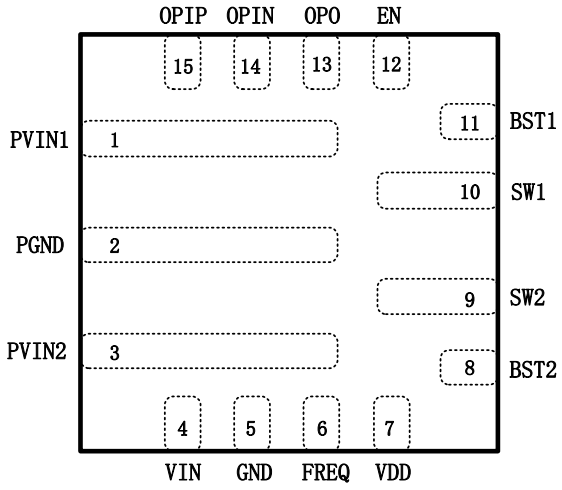


Figure 1. Top view 15-Lead QFN 3mm*3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. a local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	2	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	3	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q3. Local bypass capacitor from PVIN2 pin to PGND pin should be added. Path from PVIN2 pin to high frequency bypass capacitor and PGND must be as short as possible.

VIN	4	Input supply voltage of the 5V LDO. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	5	Ground.
FREQ	6	Frequency program pin, connect a resistor to ground to set the clock frequency of full bridge.
VDD	7	Output voltage of the 5V LDO. Connect 2.2uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage.
BST2	8	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	9	Switching node of the half-bridge FETs Q3 and Q4.
SW1	10	Switching node of the half-bridge FETs Q1 and Q2.
BST1	11	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
EN	12	Enable pin. Pull the pin high or keep it floating to enable the IC. When the device is enabled, 5V LDO will start to work if VIN higher than UVLO threshold. After VDD is established, power stage responds to clock signals.
OPO	13	Amplifier output pin.
OPIP	14	Positive input pin of Amplifier.
OPIN	15	Negative input pin of Amplifier.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	20	V
P_{VIN}	Input voltage range	1	15	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-19L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	48	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63141 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63141. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=V_{PVIN1}=V_{PVIN2}=12V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		20	V
P_{VIN}	Operating input voltage		1		15	V
V_{IN_UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		3.6 400		V mV
V_{DD_UVLO}	V_{DD} UVLO Threshold Hysteresis	V_{DD} rising		3.82 400		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		1	3	μA
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	3	uA
I_{VINQ}	Quiescent current from VIN pin	R_{FREQ}=135Kohm, SW1 and SW2 floating		1.5		mA
I_{PVINQ}	Operating current from PVIN1, PVIN2	R_{FREQ}=135Kohm, SW1 and SW2 floating		0.5		mA
ENABLE INPUT						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.1		V
Power Stage						
$R_{DSON\_Q1\ Q3}$	High-side MOSFETQ1 Q3on-resistance	V_{BST1}-V_{SW1}=5V, V_{BST2}-V_{SW2}=5V		16		mΩ
$R_{DSON\_Q2\ Q4}$	Low-side MOSFETQ2 Q4on-resistance	VDD=5V		16		mΩ
I_{LIM}	How-side current limit threshold			12.5		A
5V LDO						
V_{DD}	Output voltage	Cout=10uF	4.95	5	5.05	V
I_{DD}	Output current Capability			100		mA
Clock Generator						
F_{SW}	Clock Frequency	R_{FREQ}=135Kohm	58.8	60	61.2	KHz
		R_{FREQ}=62Kohm	130.34	133	135.66	KHz
		R_{FREQ}=241.1Kohm	32.34	33	33.66	KHz
Duty	Clock duty cycle			50		%
Operational Amplifier						
V_{CM}	Common-mode input range	VDD=5V	0.3		4.3	V
IB	Input bias current		-1		+1	uA
G	Gain*			60		dB
GBW	Bandwidth*	C_{LOAD}=100pF		600		KHz
V_{OS}	Offset voltage		-10		+10	mV
SR	Slew rate	C_{LOAD}=100pF		0.2		V/us
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 35		°C °C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

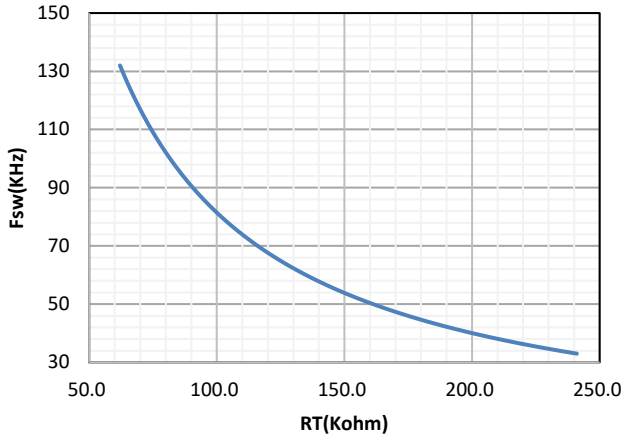


Figure 2. Clock Frequency VS FREQ Resistor

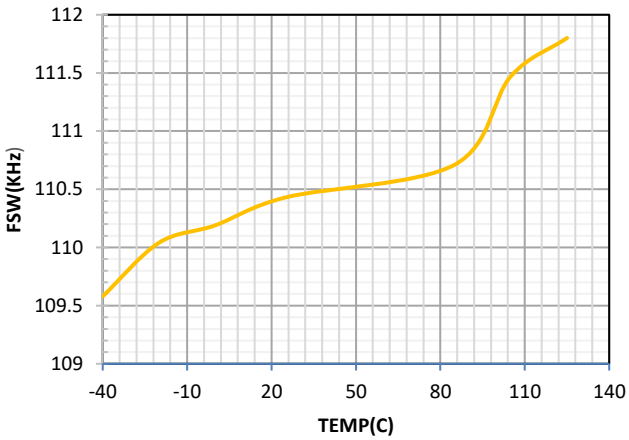


Figure 3. Frequency VS Temperature

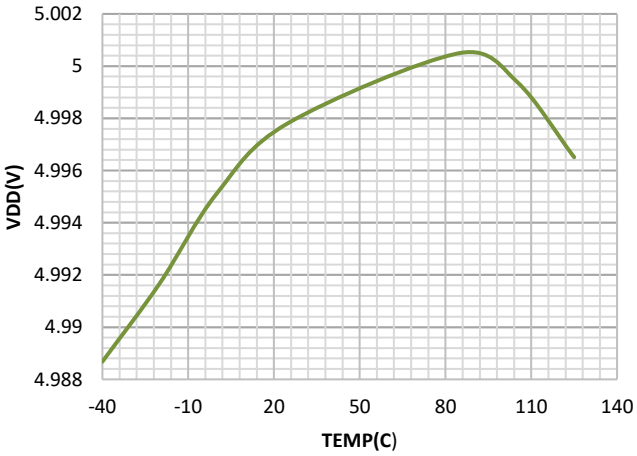


Figure 4. VDD VS Temperature

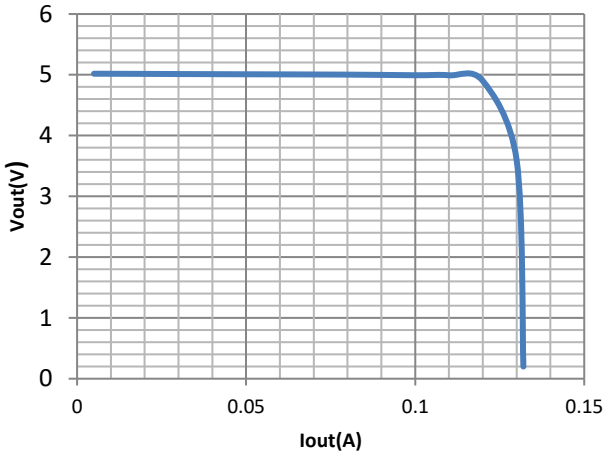


Figure 5. 5V LDO Iout vs Vout

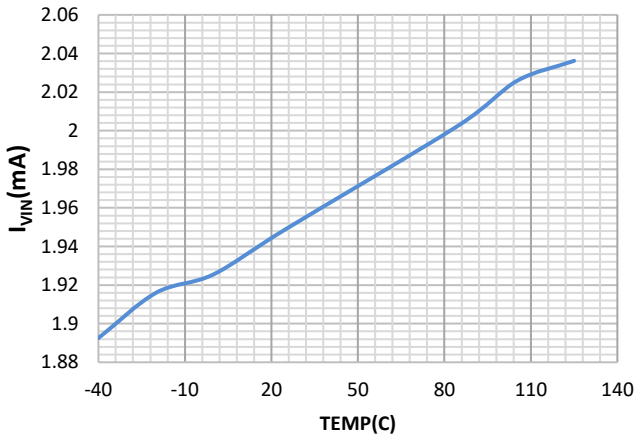


Figure 6. Input Quiescent current VS Temperature

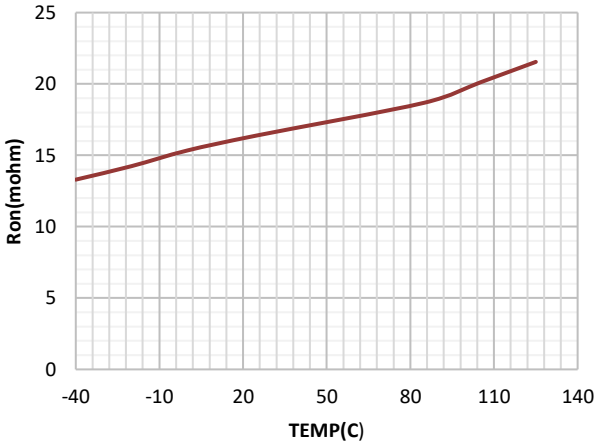


Figure 7. Full bridge Ron VS Temperature

FUNCTIONAL BLOCK DIAGRAM

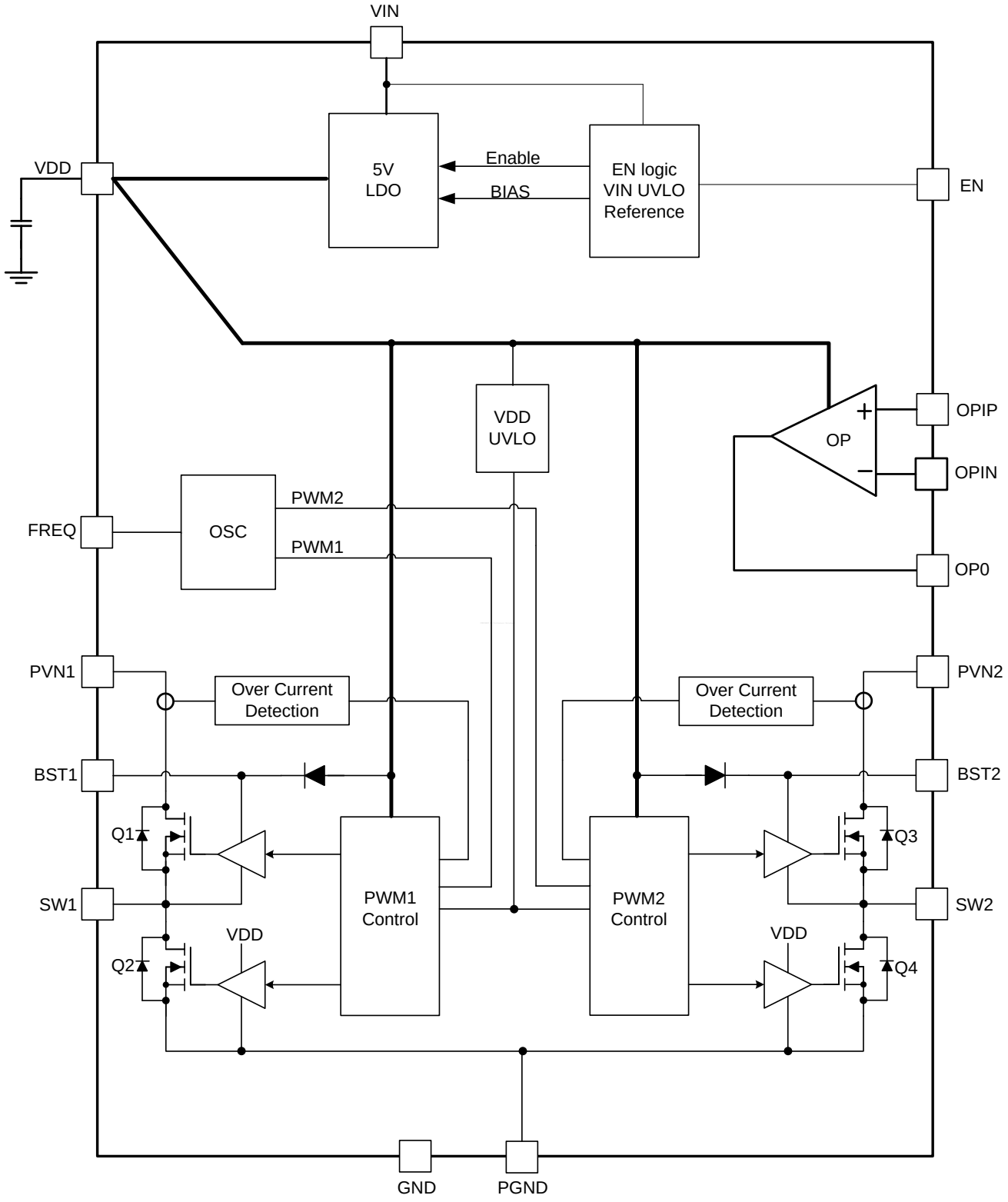


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT63141 is a highly integrated power management unit optimized for wireless power transmitter. This device integrates all of the power functions required to a wireless power transmitter including 5V output LDO, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, 50% duty clock generator with programmable frequency and amplifier for silicon photodiode signal demodulation.

The SCT63141 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-Voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 15V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

The SCT63141 integrates a high-precision oscillator which the frequency can be programmed by an external resistor. Two complementary clock signals with 50% duty cycle out from the oscillator control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. The transmitted power can be configured by adjusting the frequency of clock on the basis of the LC resonant frequency and also the power requirement from receiver.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63141 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for 5V LDO and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.2V, the 5V output LDO enables at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. Once VDD rise up to 3.8V, 4-MOSFETs full bridge allows clock signals to control for switching. Clock signal cannot control full bridge of MOSFETs if VDD drop to 3.36V.

An internal1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider (R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.2 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \quad (1)$$

$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 5.5uA * R1 \quad (2)$$

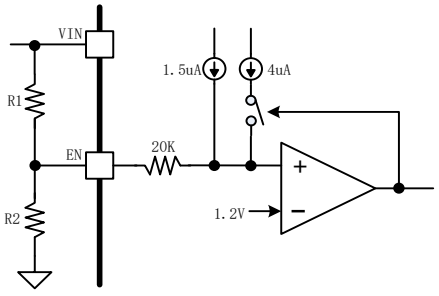


Figure9. System UVLO by enable divider

5V LDO

The SCT63141 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Clock Generator

The SCT63141 has an integrated clock generator to produce two complementary clock signals to control the full bridge power. The duty cycle of the output clock signals is fixed 50% while the frequency of the clock can be configured through an external resistor connecting from FREQ pin to GND pin. The frequency configuration range is from 33KHz to 132KHz. The transmitted power can be configured by adjusting the frequency of clock on the basis of the LC resonant frequency and also the power requirement from receiver. Use Equation 3 or the table1 to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{8100}{fsw(KHz)} * [1 + \left(133.4 - \frac{8100}{fsw(KHz)}\right) * \frac{1.6}{10000}] \quad (3)$$

Table 1. RT Resistance for Switching Frequency Selection

FOSC(KHz)	RT(Kohm)	FOSC(KHz)	RT(Kohm)	FOSC(KHz)	RT(Kohm)	FOSC(KHz)	RT(Kohm)	FOSC(KHz)	RT(Kohm)
33	**241.1**	53	**152.4**	73	**111.4**	93	**87.7**	113	**72.4**
34	**234.2**	54	**149.6**	74	**109.9**	94	**86.8**	114	**71.8**
35	**227.8**	55	**146.9**	75	**108.4**	95	**85.9**	115	**71.1**
36	**221.7**	56	**144.4**	76	**107.0**	96	**85.0**	116	**70.5**
37	**215.9**	57	**141.9**	77	**105.7**	97	**84.2**	117	**69.9**
38	**210.4**	58	**139.5**	78	**104.3**	98	**83.3**	118	**69.4**
39	**205.2**	59	**137.2**	79	**103.0**	99	**82.5**	119	**68.8**
40	**200.3**	60	**135.0**	80	**101.8**	100	**81.7**	120	**68.2**
41	**195.5**	61	**132.8**	81	**100.5**	101	**80.9**	121	**67.7**
42	**191.0**	62	**130.7**	82	**99.3**	102	**80.1**	122	**67.1**
43	**186.7**	63	**128.7**	83	**98.1**	103	**79.3**	123	**66.6**
44	**182.6**	64	**126.7**	84	**97.0**	104	**78.6**	124	**66.0**
45	**178.7**	65	**124.8**	85	**95.9**	105	**77.8**	125	**65.5**
46	**174.9**	66	**122.9**	86	**94.8**	106	**77.1**	126	**65.0**
47	**171.3**	67	**121.1**	87	**93.7**	107	**76.4**	127	**64.5**
48	**167.8**	68	**119.4**	88	**92.7**	108	**75.7**	128	**64.0**
49	**164.5**	69	**117.7**	89	**91.6**	109	**75.0**	129	**63.5**
50	**161.3**	70	**116.0**	90	**90.6**	110	**74.3**	130	**63.0**
51	**158.2**	71	**114.4**	91	**89.6**	111	**73.7**	131	**62.5**
52	**155.2**	72	**112.9**	92	**88.7**	112	**73.0**	132	**62.1**

Full bridge

The SCT63141 integrate full bridge power stage with only 16mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 33KHz to 132KHz for different applications.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

Full Bridge Over Current Protection

The SCT63141 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Operational Amplifier

The SCT63141 has an operational amplifier with two differential input pins OPIP and OPIN with OPO as the output pin. The power supply of this amplifier is VDD. Amplifier output has 8.5mA max current limit both from VDD to OPO and also from OPO to GND. The amplifier can be used as signal amplification or be configured to a comparator for silicon photodiode signal demodulation.

Thermal Shutdown

The SCT63141 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155°C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120°C, then the device restarts.

APPLICATION INFORMATION

Typical Application

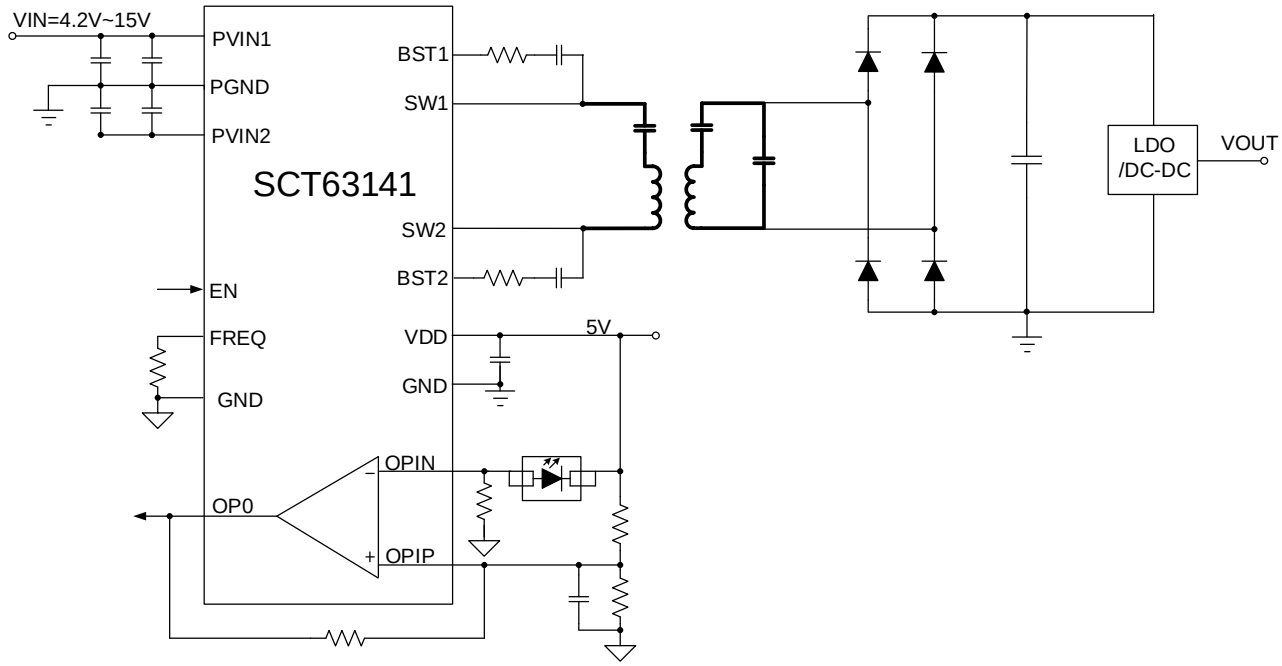


Figure 10. Wireless Power System

Application Waveforms

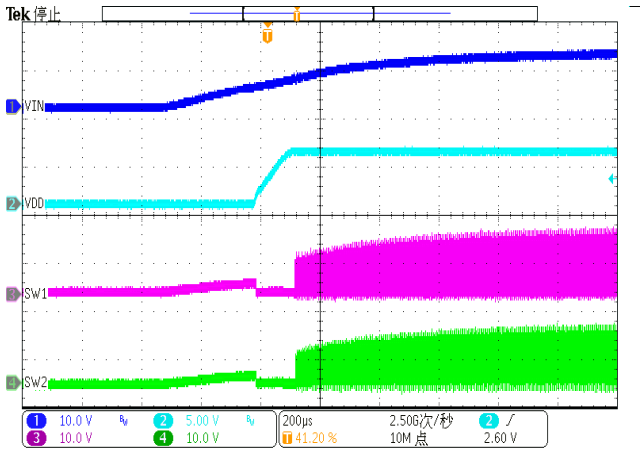


Figure 11. Power Up

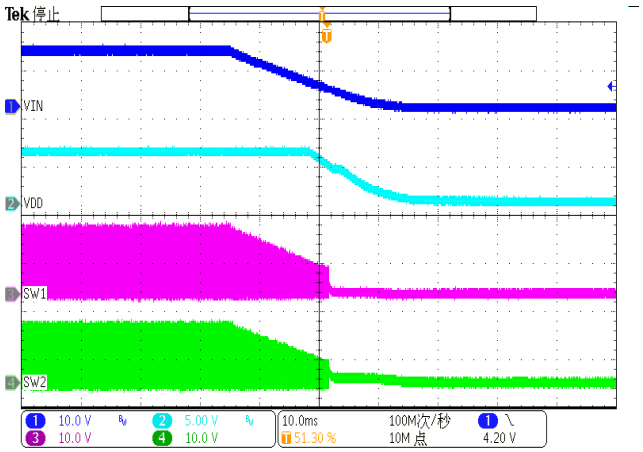


Figure 12. Power Down

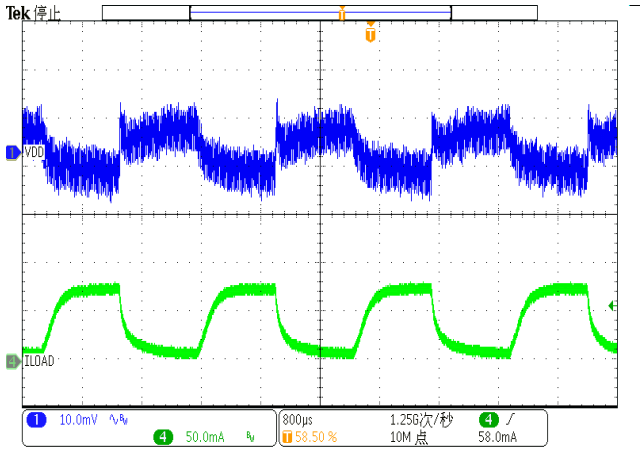


Figure 13. VDD load transient

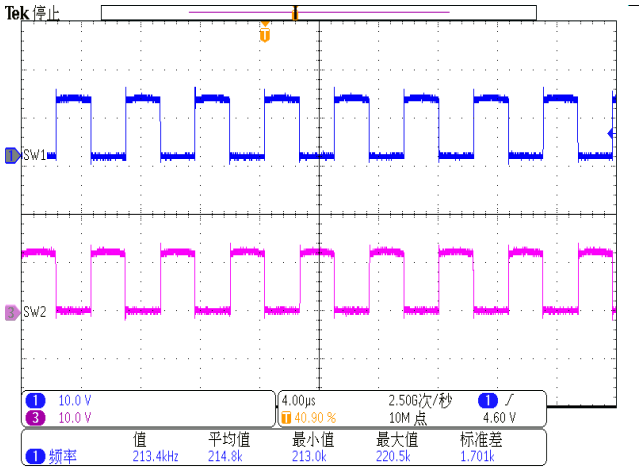


Figure 14. Full bridge

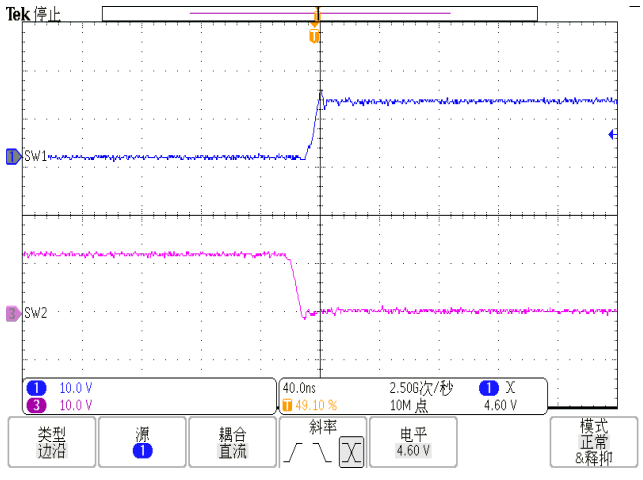


Figure 15. SW edge

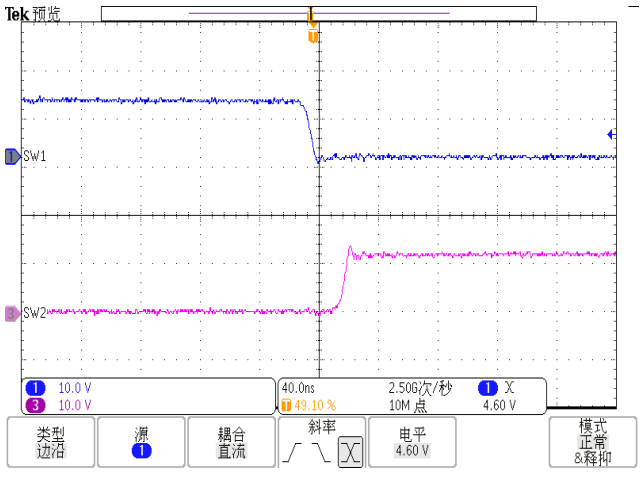


Figure 16. SW edge

Layout Guideline

Proper PCB layout is a critical for SCT63141's stable and efficient operation. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.

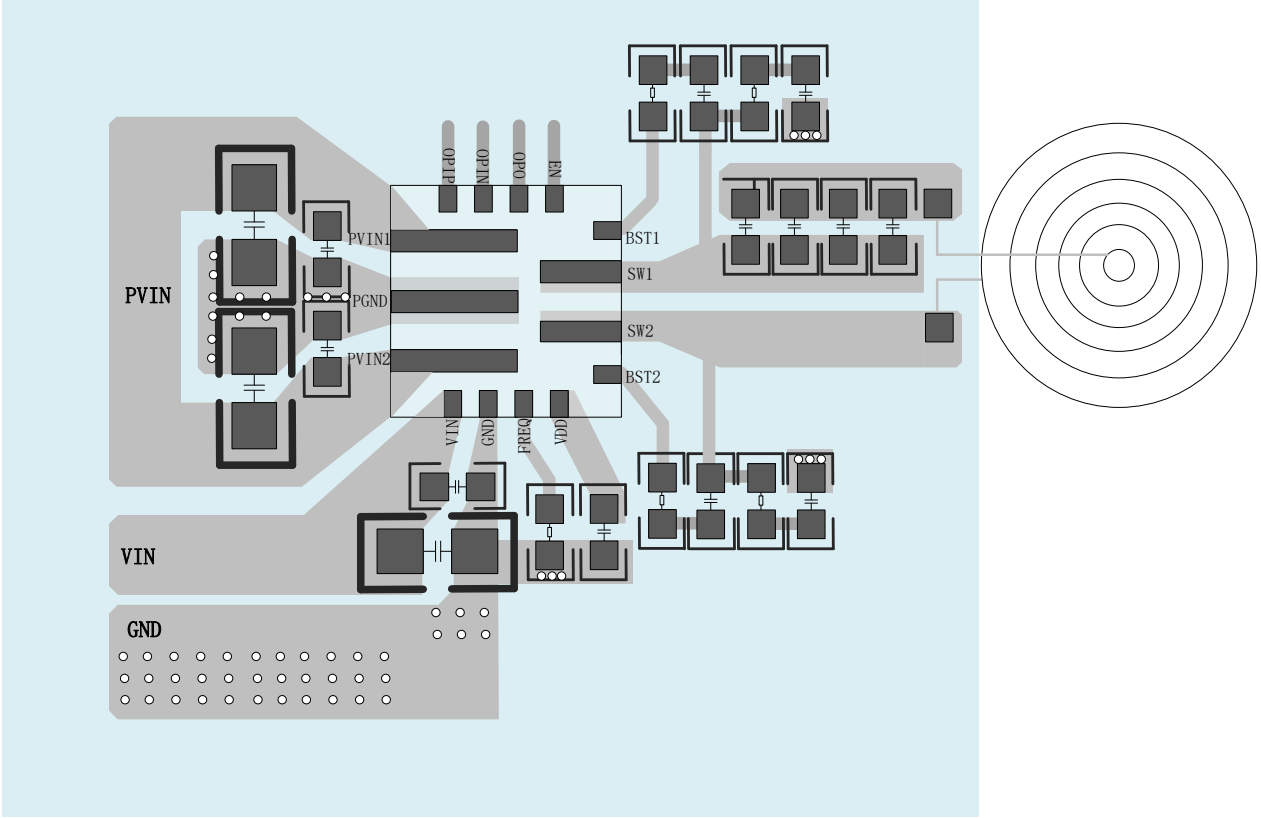
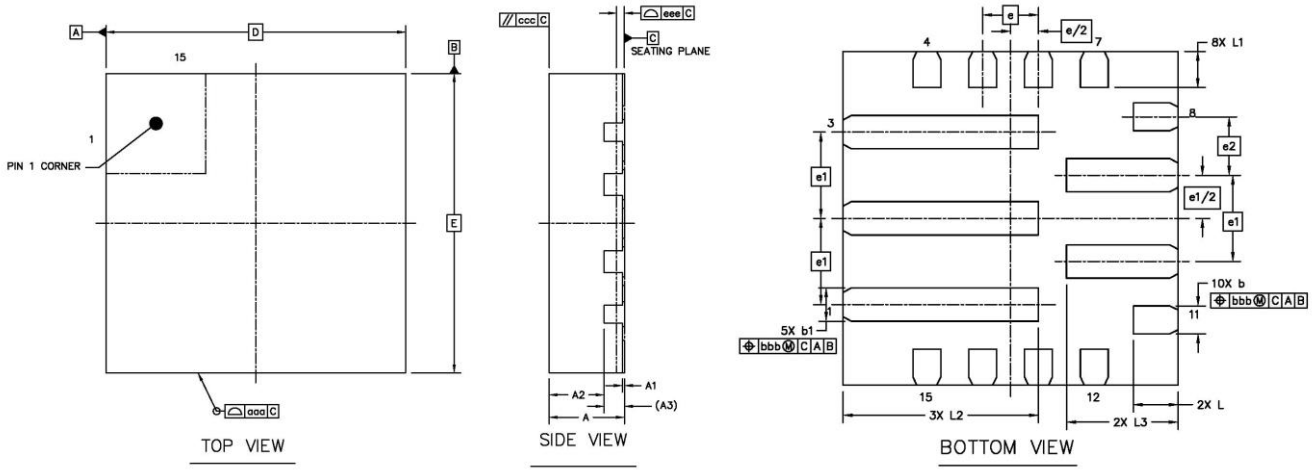


Figure 17. PCB Layout Example

PACKAGE INFORMATION



FCQFN-15L (3x3) Package Outline Dimensions

		Symbol	Dimensions in Millimeters		
			Min.	Nom.	Max.
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2		0.55	
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.20	0.25	0.30
		b1	0.25	0.30	0.35
BODY SIZE	X	D		3.00 BSC	
	Y	E		3.00 BSC	
LEAD PITCH		e		0.50 BSC	
		e1		0.775 BSC	
		e2		0.525 BSC	
LEAD LENGTH		L	0.30	0.40	0.50
		L1	0.225	0.325	0.425
		L2	1.65	1.75	1.85
		L3	0.90	1.00	1.10
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION