8.5V Vin, 2A Synchronous Step-down PPD Module™ with integrated inductor

FEATURES

- Available in a 7L ECLGA (2.5mmX1.7mm) Package
- Wide Input Voltage: 4.2V-8.5V
- 2A Continuous Output Current with Integrated 50mΩ /24mΩ FETs
- Wide Output Voltage Range:0.8V-7V
- Quiescent Current 205uA
- Cycle-by-Cycle Current Limiting
- Internal 3ms Soft-Start Limits the inrush current
- Fixed 1.2MHz Switching Frequency
- Input Under-Voltage Lockout
- Power Save Mode at light load
- Over-Temperature Protection
- Support PCB double-sided welding

APPLICATIONS

- Flat Panel Digital TV and Monitors
- Surveillance
- Set Top Boxes
- Networking Systems
- Consumer Electronics
- General Purpose

DESCRIPTION

The SCT2233M is a fully integrated high efficiency synchronous step-down DCDC converter module capable of delivering 2A current. The devices operate over a wide input voltage range from 4.2V to 8.5V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low Rdson to minimize the conduction loss.

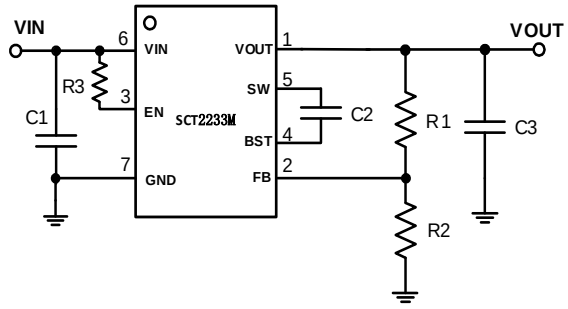
With 1.2MHz switching frequency, low output voltage ripple and small capacitor size are achieved. SCT2233M adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

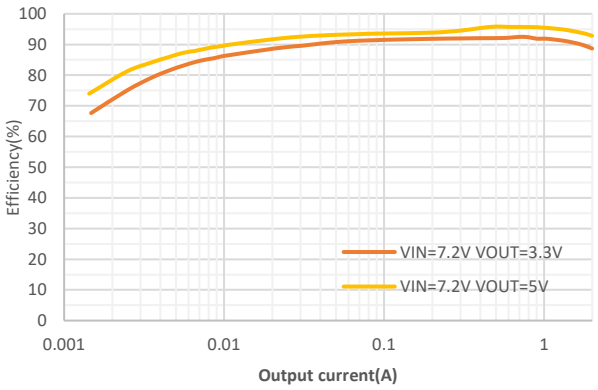
The SCT2233M operates in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2233M requires a minimal number of external components and is available in a space-saving 7L ECLGA (2.5mmX1.7mm) package.

TYPICAL APPLICATION





SCT2233M Efficiency

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Rev 1.0: Release to market

Rev 1.1: Update DEVICE ORDER INFORMATION

DEVICE ORDER INFORMATION

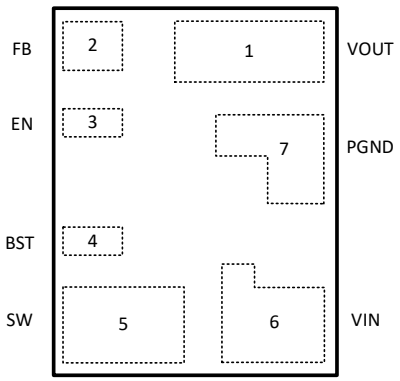
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PINS	PACKAGE DESCRIPTION
SCT2233MLUAR	Tape & Reel	5000	7	7L ECLGA (2.5mmX1.7mm)

ABSOLUTE MAXIMUM RATING

Over operating free-air temperature unless otherwise noted(1)

SYMBOL	RATING	UNIT
V_{IN}	-0.3 to 19	V
V_{SW}	-1 to 19	V
V_{SW} (<10ns)	-2.5 to 21	V
V_{BST}	V_{SW}-0.3 to V_{SW}+6	V
V_{FB}	-0.3 to 6.5	V
V_{EN}	-0.3 to 6.5	V
T_J (2)	-40 to 125	°C
T_{STG}	-65 to 150	°C

PIN CONFIGURATION



SCT2233M Top View

(2.5mm x 1.7mm)

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
VOUT	1	Power output, please use as large an output capacitor as possible to reduce output voltage ripple.
FB	2	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	3	Enable logic input. The device has precision enable thresholds 1.2V rising / 1.12V falling for programmable UVLO threshold and hysteresis.
BST	4	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
SW	5	Power Switching Output. SW is the switching node that supplies power to the output. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	6	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 8.5V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
PGND	7	Power ground. Must be soldered directly to ground plane.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	8.5	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	7L ECLGA (2.5mmX1.7mm)	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	83.16	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	86.10	
$R_{\theta JB}$	Junction to board thermal resistance(1)	14.06	
$R_{\Psi jt}$	Junction-to-top characterization parameter	18.24	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2233M are mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2233M. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=8.5V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.2		8.5	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.0 350		V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=8.5V		0.9		uA
I_Q	Quiescent current	EN=2V, No load, No switching. VIN=8.5V. BST-SW=5V		205		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.12		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			50		mΩ
R_{DSON_L}	Low side FET on-resistance			24		mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage	T_J=25°C, CCM	0.788	0.8	0.812	V
Current Limit						
I_{LIM_LSD}	LSD valley current limit		2.4	3.2	4	A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=8.5V, V_{OUT}=5V		1200		kHz
t_{ON_MIN}*	Minimum on-time			70		ns
t_{OFF_MIN}	Minimum off-time			220		ns
Soft Start Time						
t_{SS}	Internal soft-start time			3		ms
Protection						
T_{SD}*	Thermal shutdown threshold Hysteresis	T_J rising		155 25		°C

TYPICAL CHARACTERISTICS

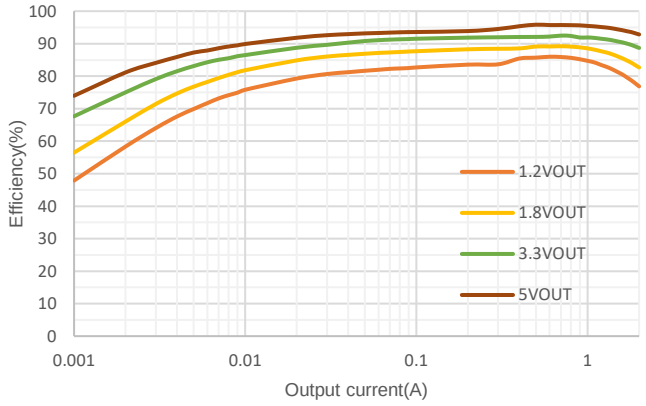


Figure 1. Efficiency vs Load Current (VIN=7.2V)

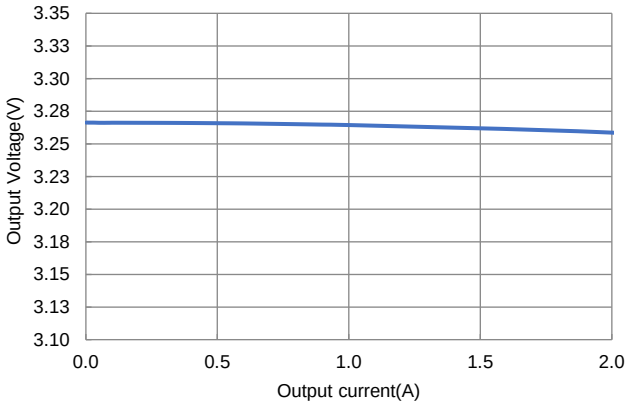


Figure 2. Load Regulation (VIN=5V)

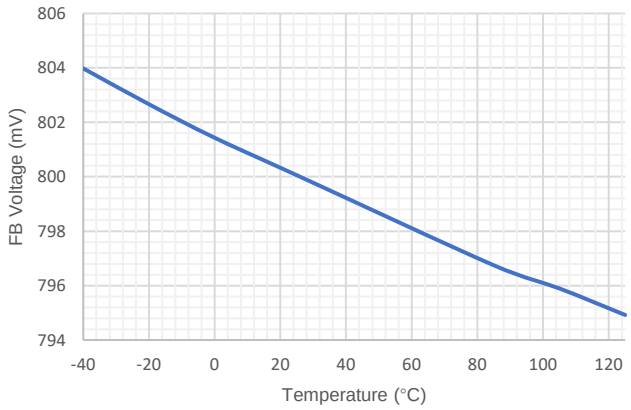


Figure 3. FB Voltage Vs. Temperature

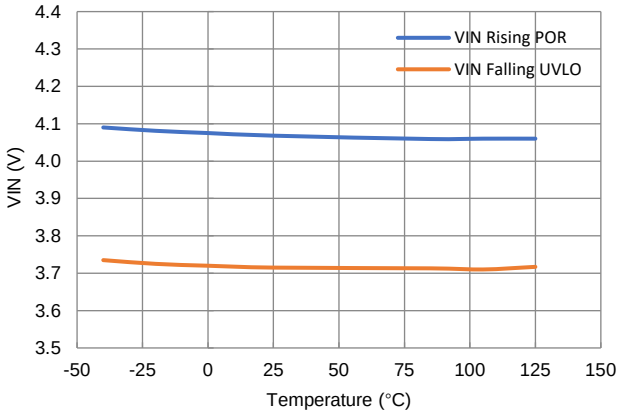


Figure 4. UVLO Vs. Temperature

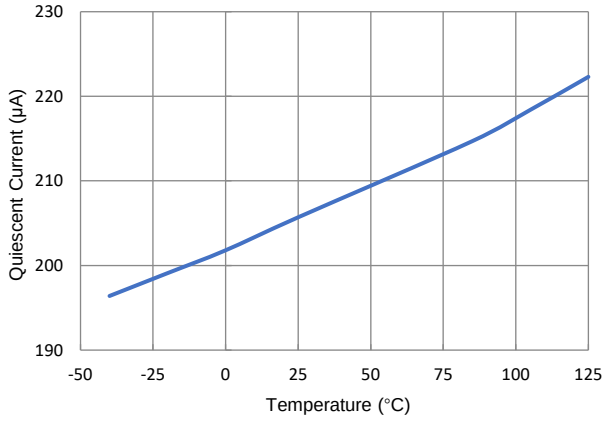


Figure 5. Quiescent Current Vs. Temperature

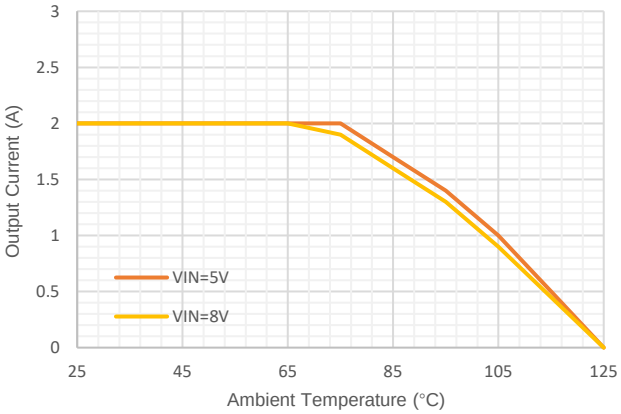


Figure 6. Thermal Derating (VOUT=1V, θ_{JA}=60°C/W)

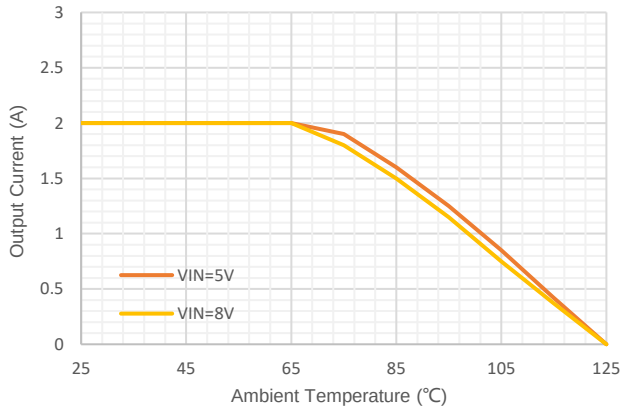


Figure 7. Thermal Derating (VOUT=1.8V, θ_{JA}=60°C/W)

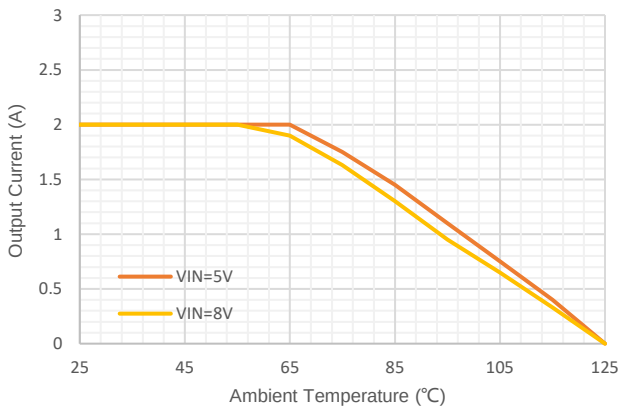


Figure 8. Thermal Derating (VOUT=3.3V, θ_{JA}=60°C/W)

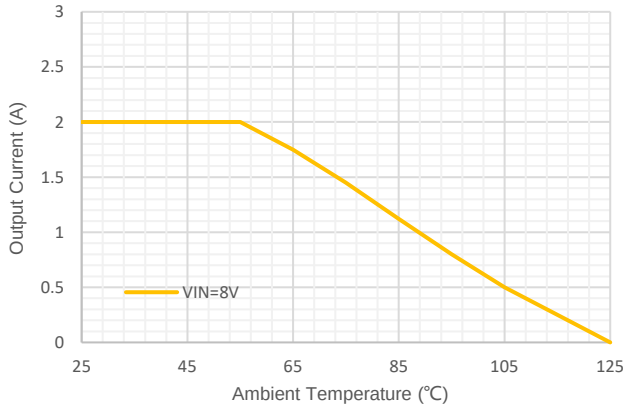
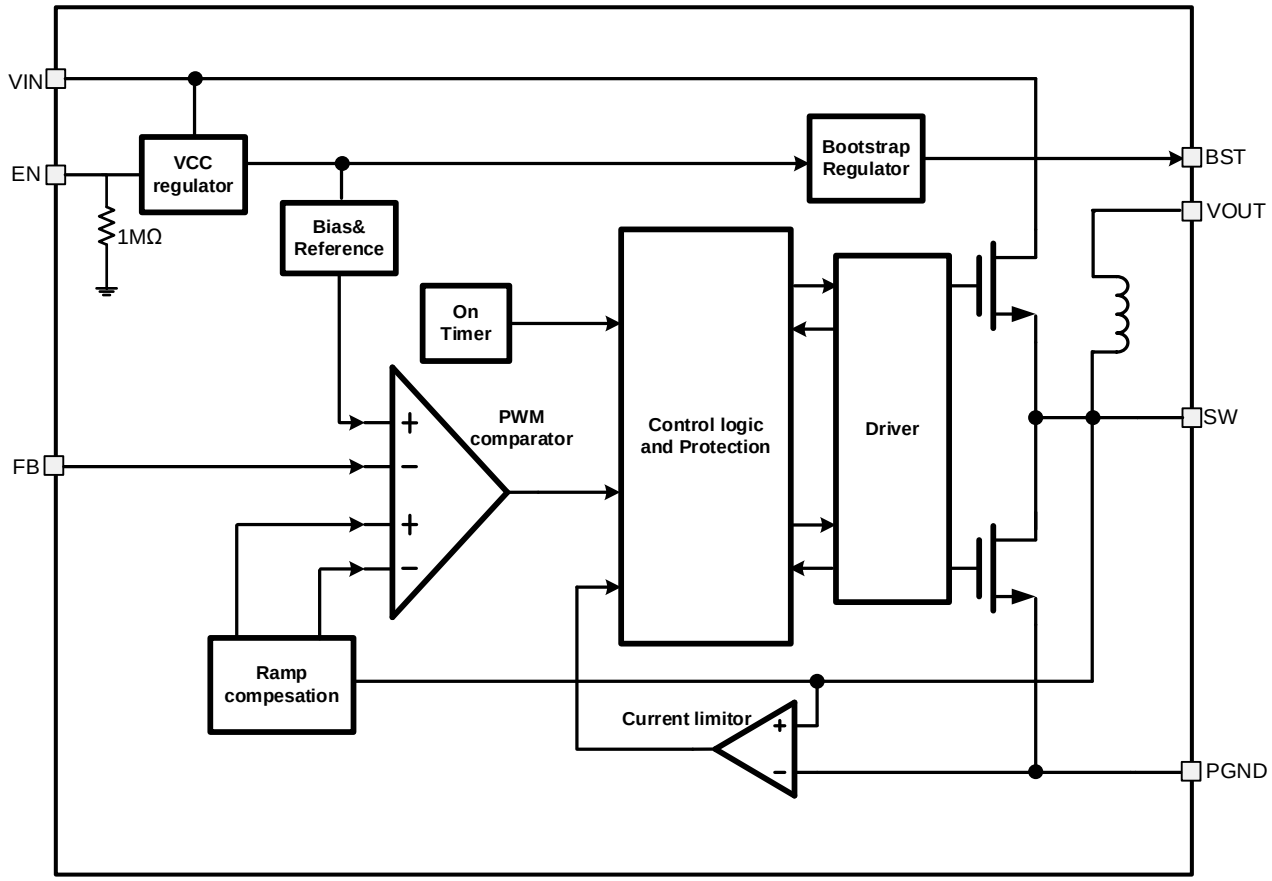


Figure 9. Thermal Derating (VOUT=5V, θ_{JA}=60°C/W)

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Adaptive On-time Control

The SCT2233M device is 4.2-8.5V input, 2A output, synchronous step-down converter module with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2233M turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2233M turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \quad (1)$$

Where:

VOUT is the output voltage.
VIN is the input voltage.
fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 220ns typical.

Power Saving Mode (PSM)

The SCT2233M is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.8V, the next ON cycle begins. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (2)$$

Where:

TON is on-time

VIN Power

The SCT2233M is designed to operate from an input voltage supply range between 4.2V to 8.5V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2233M Under Voltage Lock Out (UVLO) default startup threshold is typical 4V with VIN rising and shutdown threshold is 3.67V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT2233M enables all functions and the device starts soft-start phase. The SCT2233M has the built in 3ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.12V/fall).

An internal 1MΩ resistor from EN to GND allow EN float to shut down the chip. EN is clamped internally using a 5V series diode. For applications where a specified VIN UVLO voltage needs to be set, EN connects a resistor R3 to VIN to form a voltage divider with a 1M resistor inside the chip for the configuration of VIN UVLO voltage, as shown in Figure 10. The resistor distributor R3 is calculated by Equation (3).

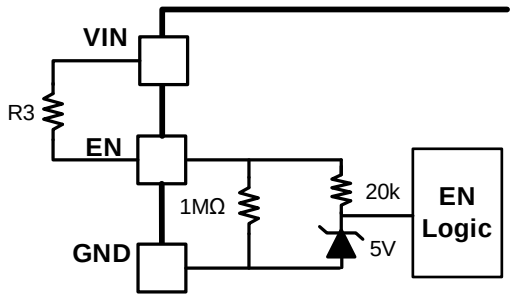


Figure 10. Adjustable VIN UVLO

$$R3 = \frac{(V_{start} - V_{ENR}) \times R}{V_{ENR}} \quad (3)$$

$$\text{Vstop} = V_{ENF} \times \frac{R + R_3}{R} \quad (4)$$

Where:

- Vstart: Vin rise threshold to enable the device
- Vstop: Vin fall threshold to disable the device
- V_{ENR}=1.2V
- V_{EMF}=1.12V
- R=1MΩ

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be

triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will drop below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Thermal Shutdown

Once the junction temperature in the SCT2233M exceeds 155°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 130°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

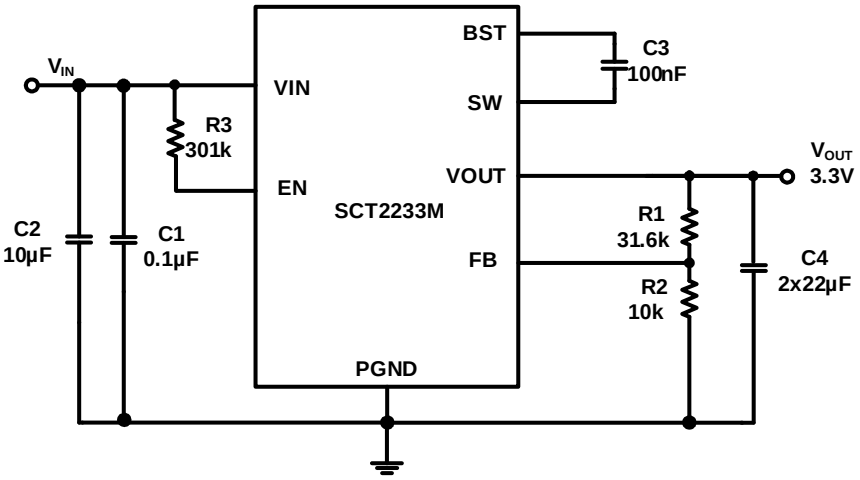


Figure 11. 8.5V Input, 3.3V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	8.5V
Output Voltage	3.3V
Output Current	2A
Switching Frequency	1.2MHz
Output voltage ripple (peak to peak)	25mV
Transient Response 0.5A to 1.5A load step	ΔVout = 120mV

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2233M.

Use Equation (5) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Feedback Resistor Divider Selection

The SCT2233M features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 11. Use equation (8) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \quad (8)$$

Table 1. Recommended Component Selections

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C2 (μF)	C4 (μF)	C3 (nF)
1.2	4.99	10.2	10	2 x 22	100
1.5	8.66	10.2	10	2 x 22	100
1.8	12.4	10.2	10	2 x 22	100
2.5	21.5	10.2	10	2 x 22	100
3.3	31.6	10.2	10	2 x 22	100
5.0	12.7	2.4	10	2 x 22	100

Application Waveforms

Vin=8.5V, Vout=3.3V, unless otherwise noted

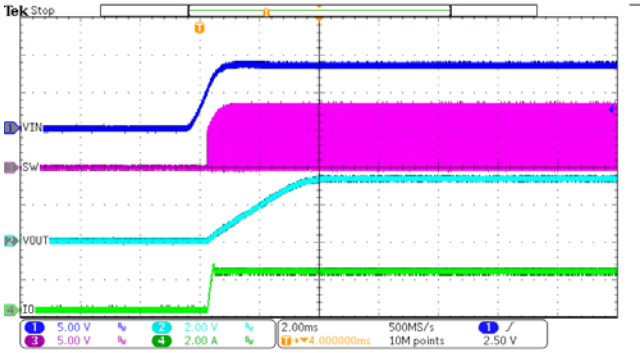


Figure 12. Power up (Iload=2A)

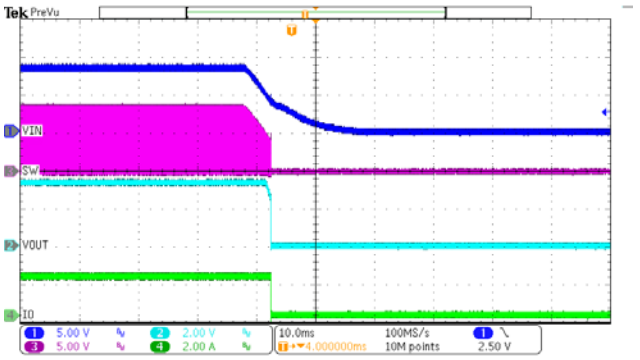


Figure 13. Power down (Iload=2A)

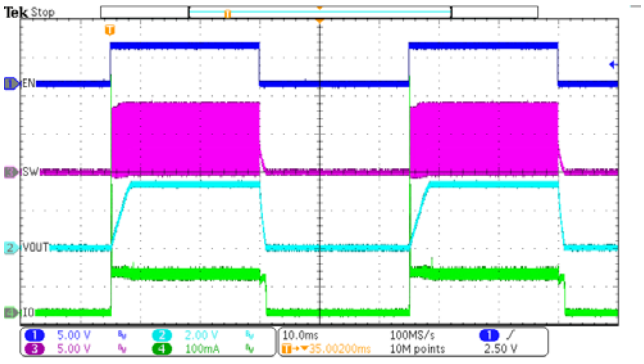


Figure 14. EN toggle (Iload=0.1A)

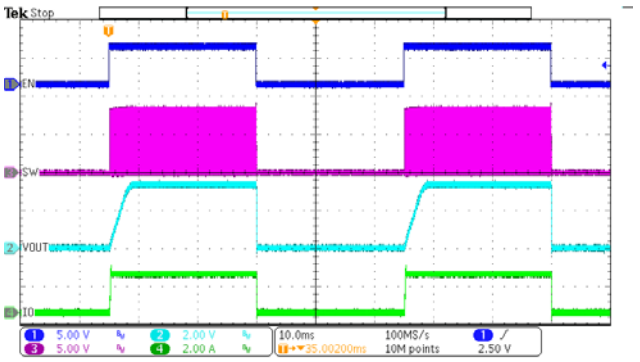


Figure 15. EN toggle (Iload=2A)

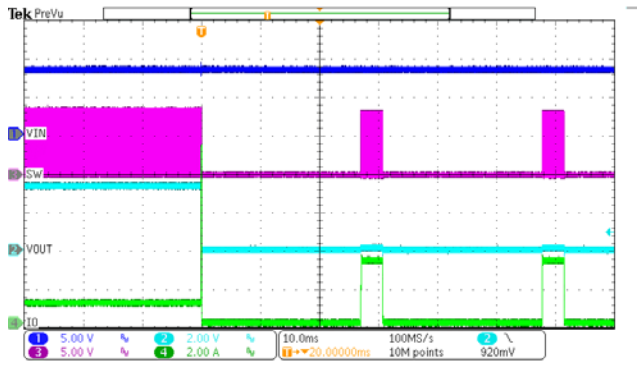


Figure 16. Over Current Protection (1A to hard short)

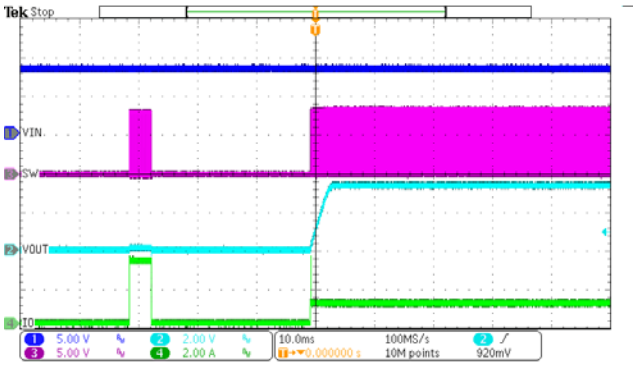


Figure 17. Over Current Release (hard short to 1A)

Application Waveforms

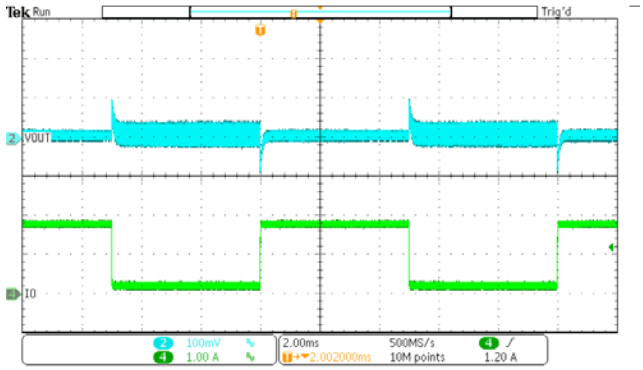


Figure 18. Load Transient (0.2A-1.8A, 0.1A/us)

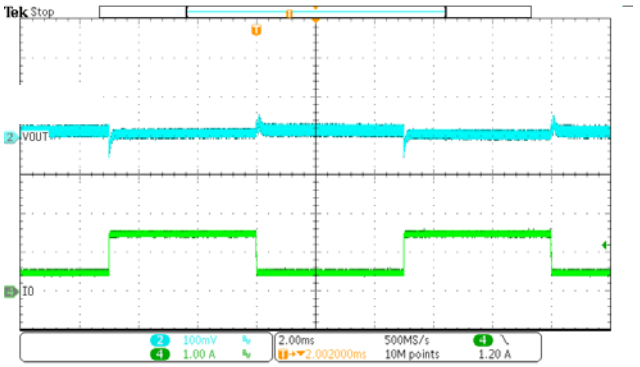


Figure 19. Load Transient (0.5A-1.5A, 0.1A/us)

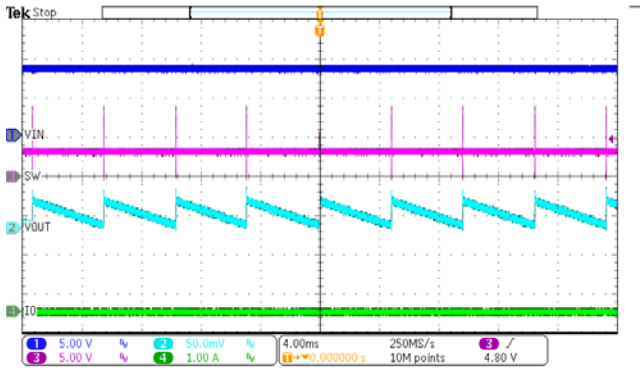


Figure 20. Output Ripple (Iload=0A)

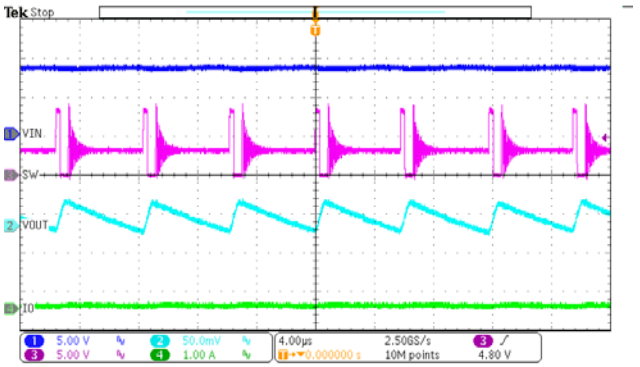


Figure 21. Output Ripple (Iload=0.1A)

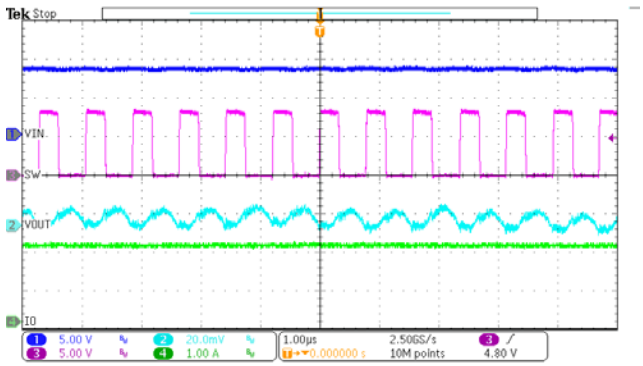


Figure 22. Output Ripple (Iload=2A)

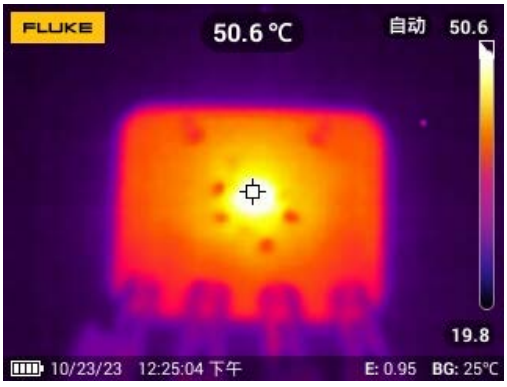


Figure 23. Thermal, 3.3Vout/2A

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 24 is the recommended PCB layout of SCT2233M.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

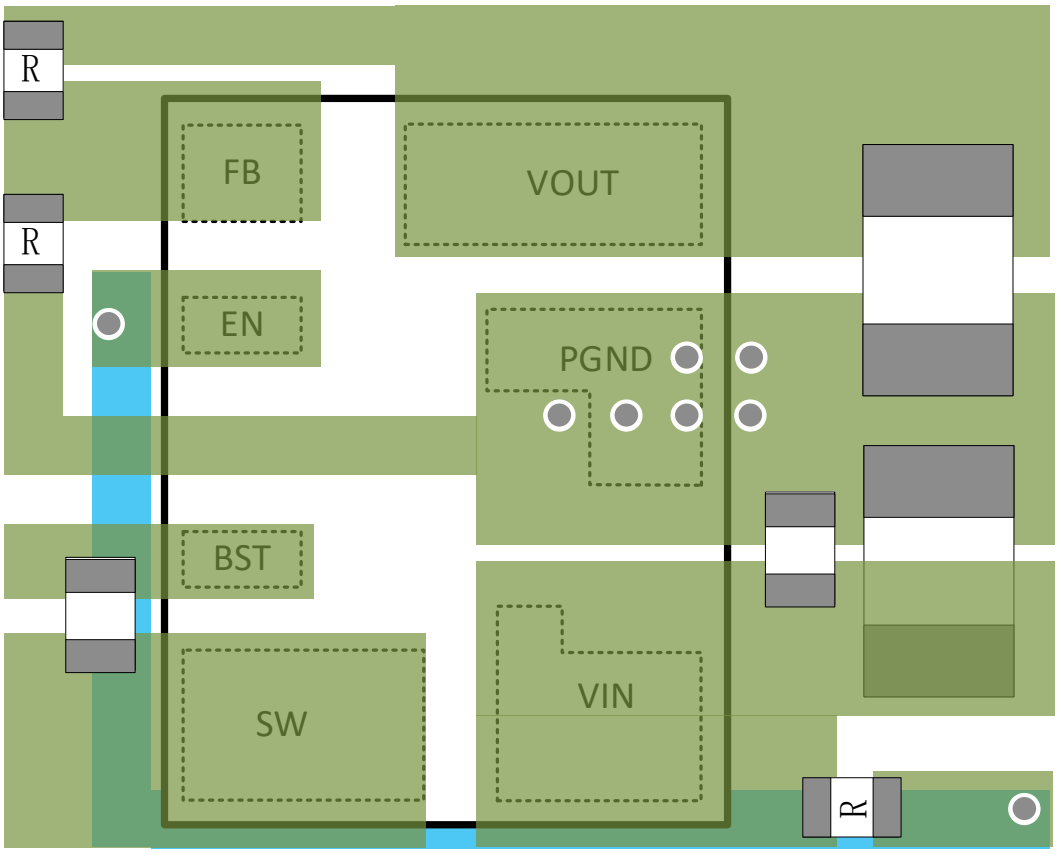


Figure 24. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (9).

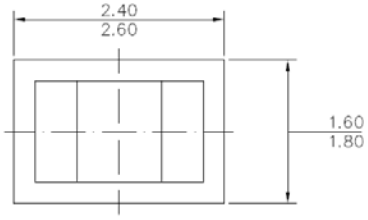
$$P_{D(MAX)} = \frac{125 - T_A}{R_{\psi JA}} \quad (9)$$

where

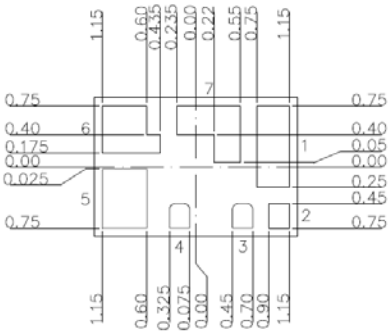
- T_A is the maximum ambient temperature for the application.
- $R_{\psi JA}$ is the junction-to-ambient thermal resistance.

The real junction-to-ambient thermal resistance $R_{\psi JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

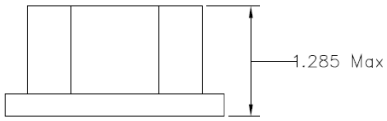
PACKAGE INFORMATION (7L ECLGA)



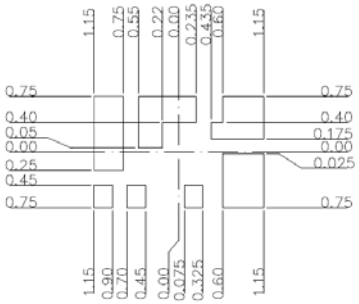
7L ECLGA TOP VIEW



7L ECLGA BOTTOM VIEW



7L ECLGA SIDE VIEW



7L ECLGA RECOMMENDED LAND PATTERN

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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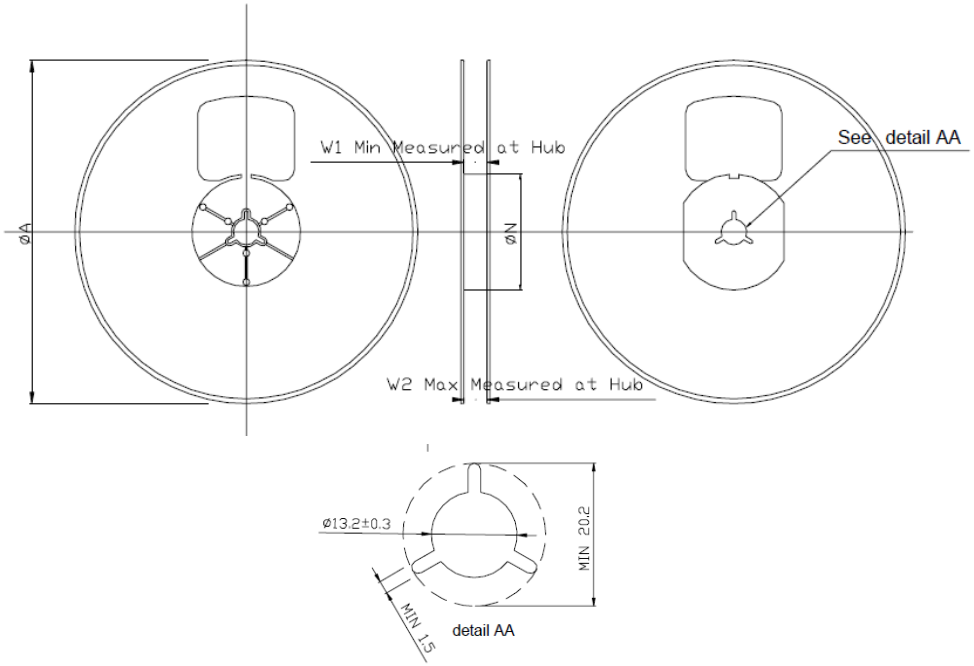
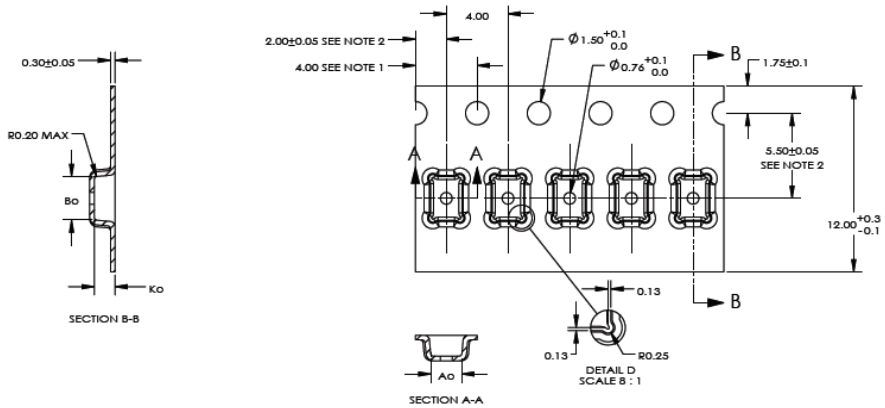
TAPE AND REEL INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
ΦA	176	178	330
ΦN	58	60	62
W1	124	-	-
W2	-	-	144
TYPE WIDTH	-	12.00	-



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
AO	1.90	2.00	2.10
BO	2.70	2.80	2.90
KO	1.3	1.35	1.45